Chapter 4
DC Biasing–BJTs
Biasing: The DC voltages applied to a transistor in order to turn it on so that it can amplify the AC signal.
Operating Point

The DC input establishes an operating or quiescent point called the Q-point.
The Three States of Operation

• **Active or Linear Region Operation**
  Base–Emitter junction is forward biased
  Base–Collector junction is reverse biased

• **Cutoff Region Operation**
  Base–Emitter junction is reverse biased

• **Saturation Region Operation**
  Base–Emitter junction is forward biased
  Base–Collector junction is forward biased
DC Biasing Circuits

- Fixed-bias circuit
- Emitter-stabilized bias circuit
- Collector-emitter loop
- Voltage divider bias circuit
- DC bias with voltage feedback
Fixed Bias
The Base-Emitter Loop

From Kirchhoff’s voltage law:

\[ +V_{CC} - I_B R_B - V_{BE} = 0 \]

Solving for base current:

\[ I_B = \frac{V_{CC} - V_{BE}}{R_B} \]
Collector-Emitter Loop

Collector current:

\[ I_C = \beta I_B \]

From Kirchhoff’s voltage law:

\[ V_{CE} = V_{CC} - I_C R_C \]
**Saturation**

When the transistor is operating in saturation, current through the transistor is at its *maximum* possible value.

\[
I_{C_{\text{sat}}} = \frac{V_{\text{CC}}}{R_C}
\]

\[
V_{CE} \approx 0 \text{ V}
\]
Load Line Analysis

The end points of the load line are:

\( I_{C_{\text{sat}}} \)
\[ I_C = \frac{V_{CC}}{R_C} \]
\[ V_{CE} = 0 \text{ V} \]

\( V_{C_{E\text{cutoff}}} \)
\[ V_{CE} = V_{CC} \]
\[ I_C = 0 \text{ mA} \]

The \( Q \)-point is the operating point:

- where the value of \( R_B \) sets the value of \( I_B \)
- that sets the values of \( V_{CE} \) and \( I_C \)
Circuit Values Affect the Q-Point

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Circuit Values Affect the Q-Point

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Circuit Values Affect the Q-Point
Emitter-Stabilized Bias Circuit

Adding a resistor (\(R_E\)) to the emitter circuit stabilizes the bias circuit.
**Base-Emitter Loop**

**From Kirchhoff’s voltage law:**

\[ + V_{CC} - I_E R_E - V_{BE} - I_E R_E = 0 \]

Since \( I_E = (\beta + 1)I_B \):

\[ V_{CC} - I_B R_B - (\beta + 1)I_B R_E = 0 \]

**Solving for \( I_B \):**

\[ I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} \]
Collector-Emitter Loop

From Kirchhoff’s voltage law:

\[ I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0 \]

Since \( I_E \approx I_C \):

\[ V_{CE} = V_{CC} - I_C (R_C + R_E) \]

Also:

\[ V_E = I_E R_E \]

\[ V_C = V_{CE} + V_E = V_{CC} - I_C R_C \]

\[ V_B = V_{CC} - I_R R_B = V_{BE} + V_E \]
Improved Biased Stability

*Stability* refers to a circuit condition in which the currents and voltages will remain fairly constant over a wide range of temperatures and transistor Beta (β) values.

Adding RE to the emitter improves the stability of a transistor.
Saturation Level

The endpoints can be determined from the load line.

\[ V_{CE \text{cutoff}}: \]
\[ V_{CE} = V_{CC} \]
\[ I_C = 0 \text{ mA} \]

\[ I_{\text{Csat}}: \]
\[ V_{CE} = 0 \text{ V} \]
\[ I_C = \frac{V_{CC}}{R_C + R_E} \]
Voltage Divider Bias

This is a very stable bias circuit.

The currents and voltages are nearly independent of any variations in $\beta$. 
Approximate Analysis

Where $I_B << I_1$ and $I_1 \approx I_2$

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2}$$

Where $\beta R_E > 10 R_2$

$$I_E = \frac{V_E}{R_E}$$

$$V_E = V_B - V_{BE}$$

From Kirchhoff’s voltage law:

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

$$I_E \approx I_C$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$
Voltage Divider Bias Analysis

Transistor Saturation Level

\[ I_{\text{Sat}} = I_{\text{Cmax}} = \frac{V_{CC}}{R_C + R_E} \]

Load Line Analysis

Cutoff:

\[ V_{CE} = V_{CC} \]
\[ I_C = 0 \text{mA} \]

Saturation:

\[ I_C = \frac{V_{CC}}{R_C + R_E} \]
\[ V_{CE} = 0 \text{V} \]
Another way to improve the stability of a bias circuit is to add a feedback path from collector to base.

In this bias circuit the Q-point is only slightly dependent on the transistor beta, $\beta$. 
**Base-Emitter Loop**

From Kirchhoff’s voltage law:

\[ V_{CC} - I'_C R_C - I_B R_B - V_{BE} - I_E R_E = 0 \]

Where \( I_B \ll I_C \):

\[ I'_C = I_C + I_B \approx I_C \]

Knowing \( I_C = \beta I_B \) and \( I_E \approx I_C \), the loop equation becomes:

\[ V_{CC} - \beta I_B R_C - I_B R_B - V_{BE} - \beta I_B R_E = 0 \]

Solving for \( I_B \):

\[ I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta (R_C + R_E)} \]
Collector-Emitter Loop

Applying Kirchoff’s voltage law:

\[ I_E + V_{CE} + I'_C R_C - V_{CC} = 0 \]

Since \( I'_C \cong I_C \) and \( I_C = \beta I_B \):

\[ I_C (R_C + R_E) + V_{CE} - V_{CC} = 0 \]

Solving for \( V_{CE} \):

\[ V_{CE} = V_{CC} - I_C (R_C + R_E) \]
Base-Emitter Bias Analysis

Transistor Saturation Level

\[ I_{C_{sat}} = I_{C_{max}} = \frac{V_{CC}}{R_C + R_E} \]

Load Line Analysis

**Cutoff:**

\[ V_{CE} = V_{CC} \]
\[ I_C = 0 \text{ mA} \]

**Saturation:**

\[ I_C = \frac{V_{CC}}{R_C + R_E} \]
\[ V_{CE} = 0 \text{ V} \]
Transistor Switching Networks

Transistors with only the DC source applied can be used as electronic switches.
Switching Circuit Calculations

Saturation current:

\[ I_{C\text{sat}} = \frac{V_{CC}}{R_C} \]

To ensure saturation:

\[ I_B > \frac{I_{C\text{sat}}}{\beta_{dc}} \]

Emitter-collector resistance at saturation and cutoff:

\[ R_{\text{sat}} = \frac{V_{CE\text{sat}}}{I_{C\text{sat}}} \]

\[ R_{\text{cutoff}} = \frac{V_{CC}}{I_{CEO}} \]
Switching Time

Transistor switching times:

\[ t_{\text{on}} = t_r + t_d \]

\[ t_{\text{off}} = t_s + t_f \]
Troubleshooting Hints

• Approximate voltages
  – $V_{BE} \approx 0.7 \text{ V}$ for silicon transistors
  – $V_{CE} \approx 25\% \text{ to } 75\% \text{ of } V_{CC}$

• Test for opens and shorts with an ohmmeter.

• Test the solder joints.

• Test the transistor with a transistor tester or a curve tracer.

• Note that the load or the next stage affects the transistor operation.
PNP Transistors

The analysis for $pnp$ transistor biasing circuits is the same as that for $nnp$ transistor circuits. The only difference is that the currents are flowing in the opposite direction.